

Appl. No.: 10/680,769
Amdt. dated April 27, 2005
Second Reply to Office Action of December 29, 2004

AMENDMENT

Amendments to the Claims:

Please amend the claims to read as follows:

1.-5. (Canceled)

6. (Currently amended) ~~The motor of claim 1;~~ An electrical motor that comprises:

a rotor having multiple magnetic poles;

a stator having multiple windings configurable to exert a torque on the rotor when energized in a commutational sequence; and

a semiconductor on insulator (SOI) application-specific integrated circuit (ASIC) coupled to the windings of the stator and configured to apply the commutational sequence,

wherein the SOI ASIC is configured to receive signals indicative of back EMF polarity on undriven windings of the stator to perform directional zero crossing detection, wherein the SOI ASIC determines the commutational sequence based on those zero crossings that only occur in anticipated directions, and

wherein the SOI ASIC includes one or more limit inputs configured to halt advancement of the commutational sequence in a predetermined direction.

7. (Original) The motor of claim 6, wherein the SOI ASIC further includes a direction input to indicate whether the commutational sequence should be advance in a forward or reverse direction when a commutation event occurs.

8.-9. (Canceled)

10. (Currently amended) ~~The controller of claim 8;~~ A brushless DC motor controller that comprises:

a set of comparators each configured to determine a voltage polarity on a respective winding of a stator; and

Appl. No.: 10/680,769
Amtd. dated April 27, 2005
Second Reply to Office Action of December 29, 2004

a clocked digital circuit configured to receive polarity signals from the comparators, configured to detect in the polarity signals zero crossings having expected crossing directions, and configured to determine a commutational sequence for energizing windings on the stator based at least in part on zero crossings, but only those zero crossings having the expected crossing directions,

wherein the clocked digital circuit samples a polarity signal before a lockout period and compares the sample to the polarity signal after the lockout ends, and wherein the clocked digital circuit generates a zero crossing indication if the sample does not match the polarity signal after the lockout ends.

11. (Currently amended) ~~The controller of claim 8,~~ A brushless DC motor controller that comprises:

a set of comparators each configured to determine a voltage polarity on a respective winding of a stator; and

a clocked digital circuit configured to receive polarity signals from the comparators, configured to detect in the polarity signals zero crossings having expected crossing directions, and configured to determine a commutational sequence for energizing windings on the stator based at least in part on zero crossings, but only those zero crossings having the expected crossing directions, wherein the clocked digital circuit includes:

a first counter configured to count a number of cycles of a clock signal between detected zero crossings of the polarity signals; and

a second counter configured to receive a count from the first counter and to count down from said count at approximately twice the rate of the clock signal, and

wherein the clocked digital circuit is configured to advance the commutational sequence when the second counter rolls over.

12. (Currently amended) ~~The controller of claim 8,~~ A brushless DC motor controller that comprises:

Appl. No.: 10/680,769
Amdt. dated April 27, 2005
Second Reply to Office Action of December 29, 2004

a set of comparators each configured to determine a voltage polarity on a respective winding of a stator; and
a clocked digital circuit configured to receive polarity signals from the comparators, configured to detect in the polarity signals zero crossings having expected crossing directions, and configured to determine a commutational sequence for energizing windings on the stator based at least in part on zero crossings, but only those zero crossings having the expected crossing directions,
wherein the clocked digital circuit accepts one or more limit inputs and is configured to inhibit advancement of the commutational sequence in a direction associated with the limit signal.

13. (Original) A method of driving windings in a DC motor, the method comprising:
receiving with a clocked digital circuit, polarity signals indicative of whether voltages on windings of the DC motor exceed a threshold voltage, wherein the clocked digital circuit is configured to operate in temperatures exceeding 150°C;
measuring intervals between transitions of the polarity signals in predicted directions; and
advancing a commutation state at a delay of some fraction of measured intervals after transitions of the polarity signals.
14. (Original) The method of claim 13, wherein said fraction is approximately one half, and wherein the measured intervals used to determine the delay are the intervals measured immediately preceding each advancement of the commutation state.
15. (Original) The method of claim 13, wherein the clocked digital circuit comprises semiconductor on insulator (SOI) circuitry.
16. (Original) The method of claim 13, further comprising:
receiving with the clocked digital circuit a direction signal indicative of a desired motor direction, and one or more limit signals each associated with a respective motor direction; and

Appl. No.: 10/680,769
Amdt. dated April 27, 2005
Second Reply to Office Action of December 29, 2004

inhibiting advancement of the commutation state if a limit signal that is associated with a direction indicated by the direction signal is asserted.

17. (Original) The method of claim 13, wherein said measuring intervals is performed with a counter operating at a first clock rate, and wherein said delay is determined by a second counter operating at a second clock rate that is greater than the first.

18. (Original) The method of claim 17, wherein said advancing a commutation state occurs when the second counter rolls over.

19.-25. (Canceled)

26. (Currently amended) ~~The device of claim 21,~~ An integrated device that comprises:

a processor core; and

an integrated motor controller coupled to the processor core by an internal bus,

wherein the integrated motor controller is configured to receive signals indicative of back

EMF polarity on undriven windings of a DC motor to perform directional zero

crossing detection, wherein the integrated motor controller determines a

commutational sequence based on those zero crossings that only occur in

anticipated directions, and

wherein the integrated motor controller includes one or more limit inputs configured to halt advancement of a commutational sequence in a predetermined direction.

27. (Original) The device of claim 26, wherein the integrated motor controller further includes a direction input to indicate whether the commutational sequence should be advance in a forward or reverse direction when a commutation event occurs.

28.-32. (Canceled)

Appl. No.: 10/680,769
Amdt. dated April 27, 2005
Second Reply to Office Action of December 29, 2004

33. (Previously presented) The method of claim 13, wherein the clocked digital circuit is implemented in a single programmable logic device.